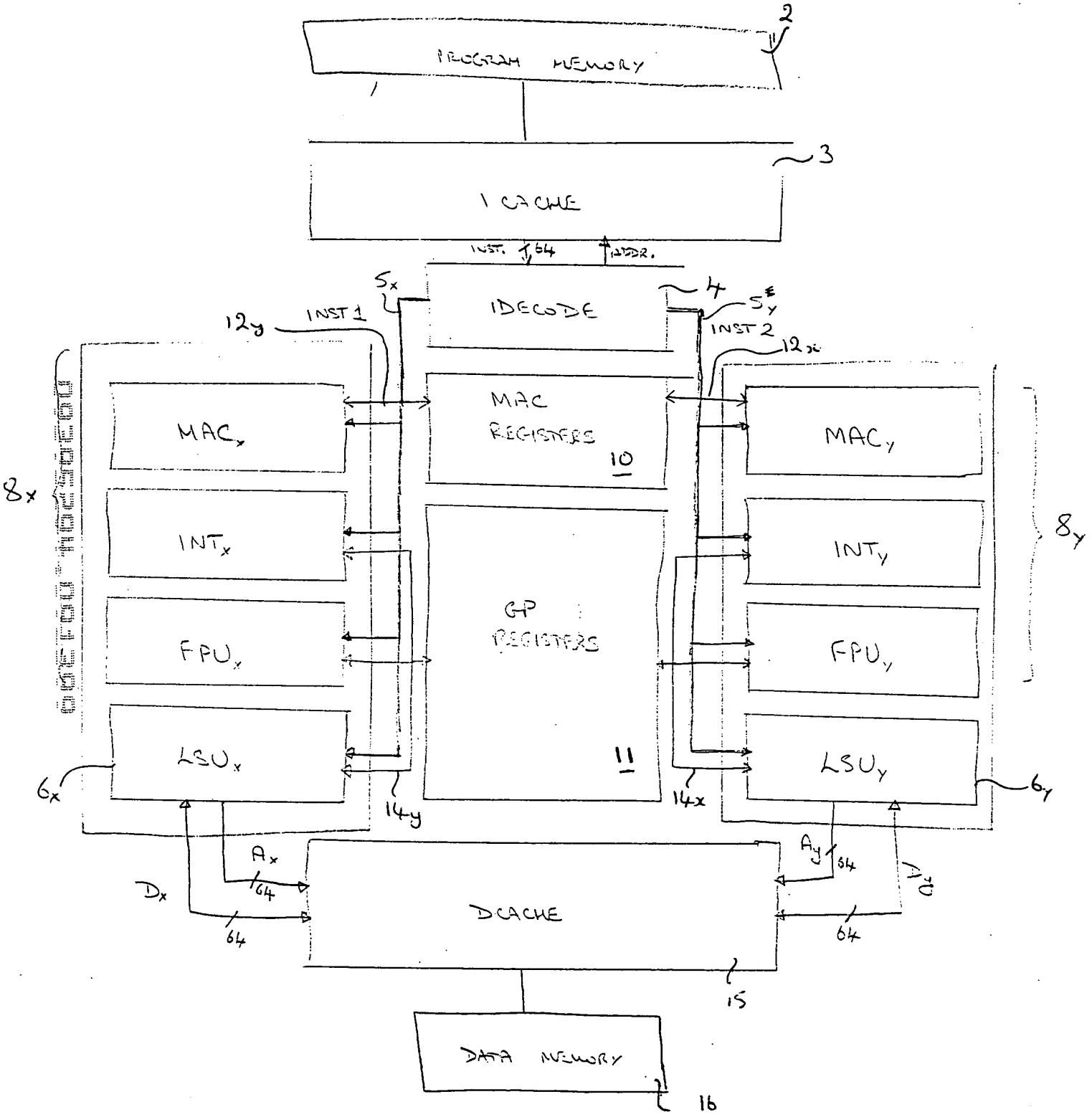
PROGRAM MEMORY
2
3
I CACHE
INST. 64
ADDR.
IDECODE
4
5x
5y
INST 1
INST 2
12y
12x
MAC REGISTERS
10
MACx
MACy
INTx
INTy
GP REGISTERS
11
FPUx
FPUy
LSUx
LSUy
8x
8y
6x
6y
14y
14x
Ax
Ay
64
Dx
Dy
DCACHE
15
DATA MEMORY
16

Figure 1

Figure 3

IDbit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
M	G		OPCODE							S	TST		SRC2					SRC1					DST								(1)
M	G		OPCODE							TST			IMMED					SRC1					DST								(2)
M	G		OPCODE							S	TST		SRC2					SRC1				SIGN		M REG							(3)
M	G		OPCODE							S	TST		SHIFT		M REG			SRC1					DST								(4)
M	G		OPCODE							S	TST		SRC2					SRC1					DST								(5)
M		OPCODE					T		IMMEDIATE OFFSET									BASE REG					DST								(6)
M		OPCODE						INDX OP			T		INDX REG					BASE REG					DST								(7)

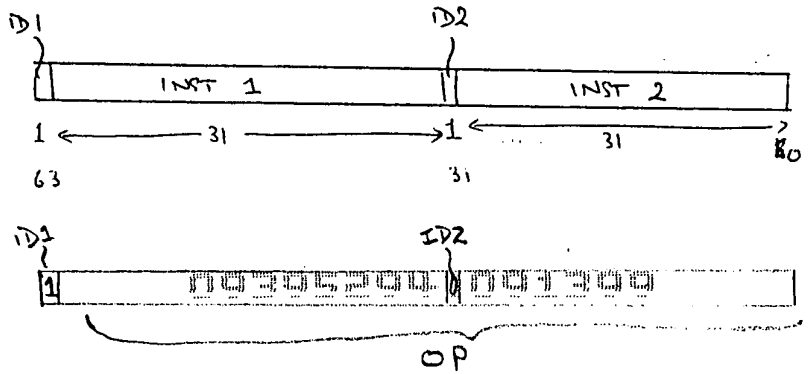

Figure 2a

Figure 2b

bit	31(M)	30(G)	29(G)
register/immediate	1	0	X
register/register	1	1	0
MAC operations	1	1	1

FIGURE 4

```
-63-62---------53--50-49-44-43-38-37--32-31-29-28-----18-17-12-11--6-5------0-
|0 |Operation | Branch condition |Immed |111 |  Immediate              | Reg   |   L1
-------------------------------------------------------------------------------
|0 |Operation |S|TST |Src4 |Src3 |Dest2 |111 |Reserved  |Src2 |Src1 | Dest1 |   L2
-------------------------------------------------------------------------------
|0 |Operation |S|TST |Immediate hi16|     |111 |Immediate lo16| Src1 | Dest1 |   L3
-------------------------------------------------------------------------------
```

Figure 5